

ArduCam IMX519 module and Terasic FPGA Board



User Manual

FPGA

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Chapter 1

Overview

This manual provides a comprehensive guide for connecting the 16MP IMX519 MIPI CSI-2 Camera Module to Terasic FPGA boards which have MIPI connectors. It covers the hardware connection setup, and a basic demo application for image acquisition.

The MIPI CSI-2 interface is a high-speed serial interface commonly used for image sensor communication. The 16MP IMX519 camera module offers high-resolution image capture, making it suitable for various applications such as machine vision, robotics, and surveillance.

Terasic FPGA boards provide a flexible platform for developing custom image processing systems. The Comet A13 Kit feature MIPI connectors, enabling easy integration of the camera module.

This manual will walk you through the steps of connecting the camera module to the FPGA board, configuring the FPGA to interface with the camera, and providing a simple demo application to capture images.

By following this manual, users will be able to successfully integrate the 16MP IMX519 camera module into their FPGA-based designs and develop custom image processing applications.

Chapter 2

Camera Module Specification

2.1 Features

Figure 2-1 shows a photograph of the camera module.



Figure 2-1 The photograph of the camera module

Table 2-1 lists the features of the camera module.

Table 2-1 The features of the camera module

Image Sensor	IMX519
Resolution	16MP
Optical Size	1/2.53"
Active Pixels	4656(H) × 3496(V)
Pixel Size	1.22μm × 1.22μm
CSI-2 Data Output	2-lane mode
Shutter Type	Rolling Shutter
Color Filter Array	Quad-Bayer RGB
Frame Rate	4656x3496@10fps, 3840x2160@21fps, 1920x1080@60fps, 1280x720@120fps
Output Format	Raw 10
F.NO	F1.75

Focus Type	Auto Focus
Focal Length	4.28mm
Field of View(FOV)	80°(D)
IR Sensitivity	Integral IR-cut Filter
Camera Board Size	24 x 25mm
Compatibility	● Terasic Comet A13 Kit ● Terasic Comet A65 Kit ● Terasic Atum A5 board ● Terasic DE25-Standard board ● Terasic DE25-Nano

- Connect Comet A13 Kit.

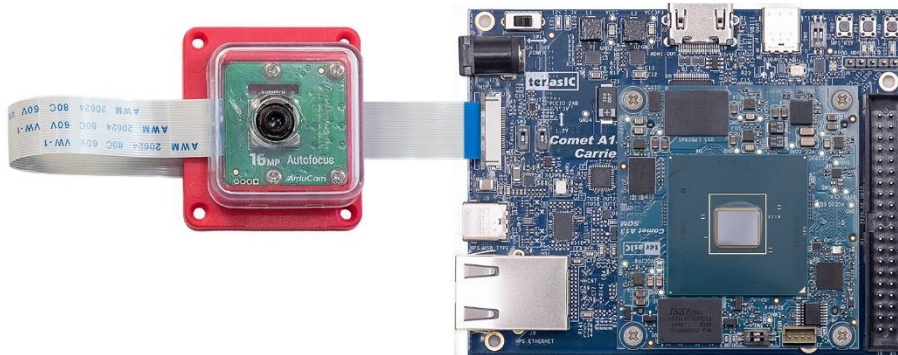


Figure 2-2 Connect to Comet A13 Kit

- Connect Comet A65 Kit.

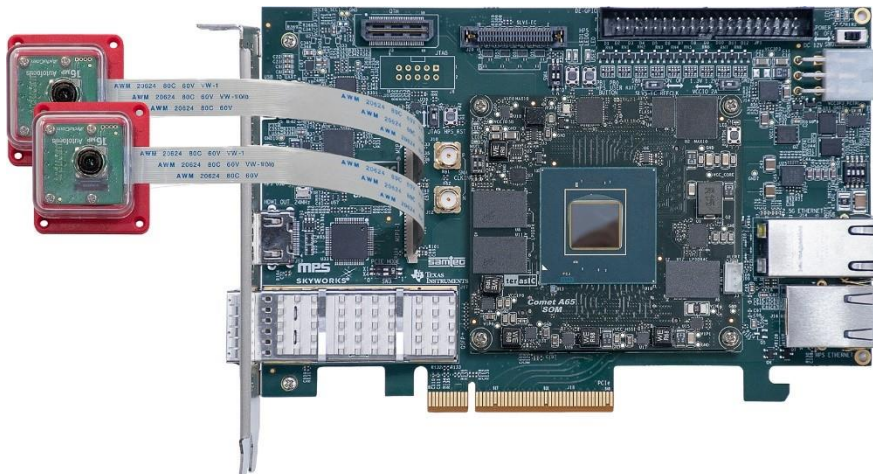


Figure 2-3 Connect to Comet A65 Kit

- Connect ATUM A5.

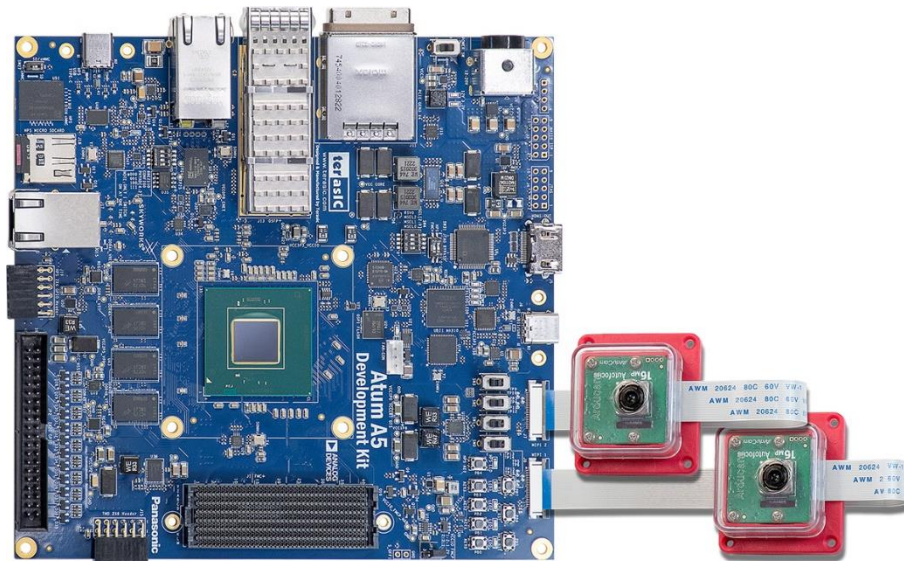


Figure 2-4 Connect to Atum A5 board

- Connect DE25-Standard.

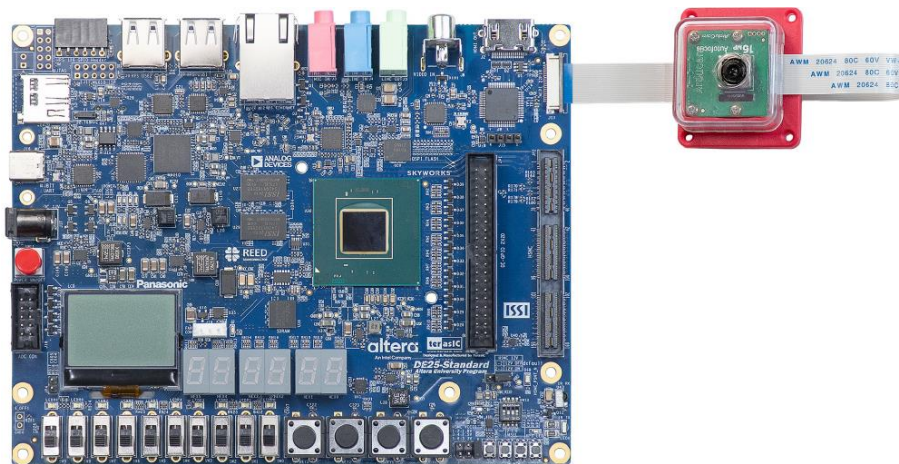


Figure 2-5 Connect to DE25-Standard board

- Connect DE25-Nano.



Figure 2-6 Connect to DE25-Nano board

Chapter 3

Camera connection setup

This chapter will guide you through the process of connecting the camera module to the Terasic FPGA development board using an FPC cable.

3.1 Connecting the Camera Module to the Terasic FPGA Board

1. As shown in the figure below, use your fingernail or a small tool to gently open the FPC connector's slider-lock. (Here we use **DE25-Standard** board as example, user may need to remove the top plastic cover of the board.)

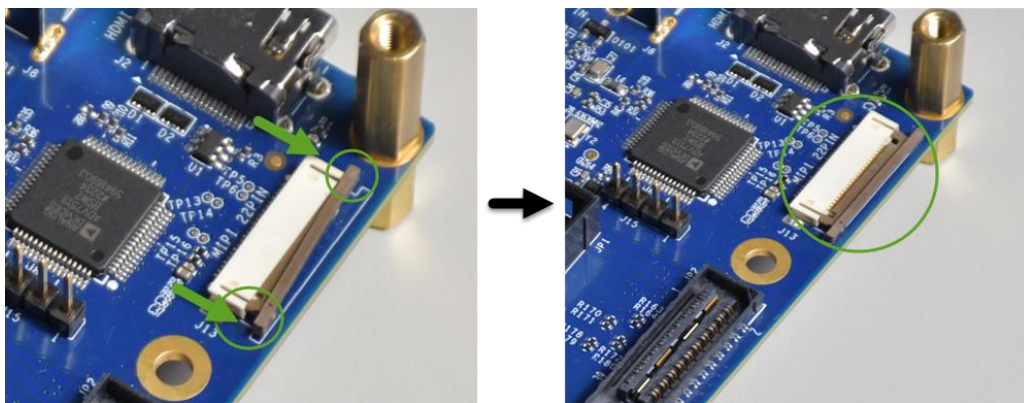


Figure 3-1 Open the slider-lock of the FPC connector

1. As shown in the figure below, hold the 22-22 pin FPC cable by its edges and align the conductive contacts with the pins of the connector. When inserting the cable, the board should be facing up and the silver contacts should be facing down.

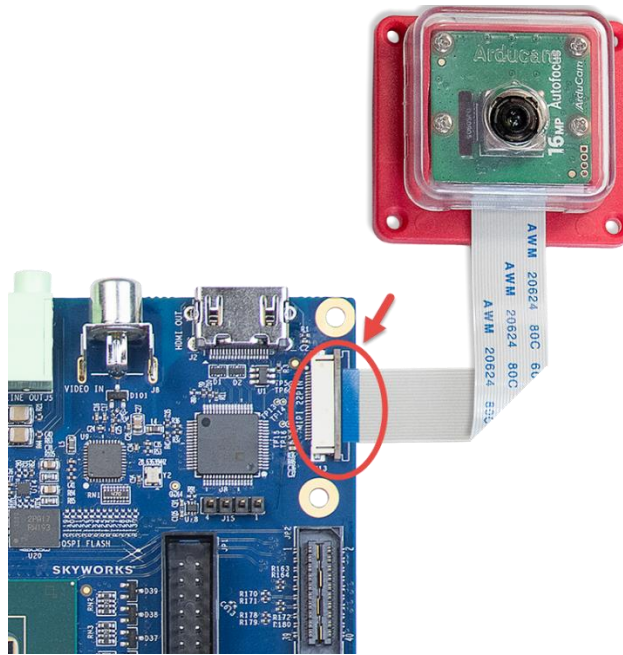


Figure 3-2 Insert the cable

2. Carefully insert the cable straight into the connector's slot. Push it in gently until it reaches the end, ensuring it is seated evenly without bending or damaging the cable.

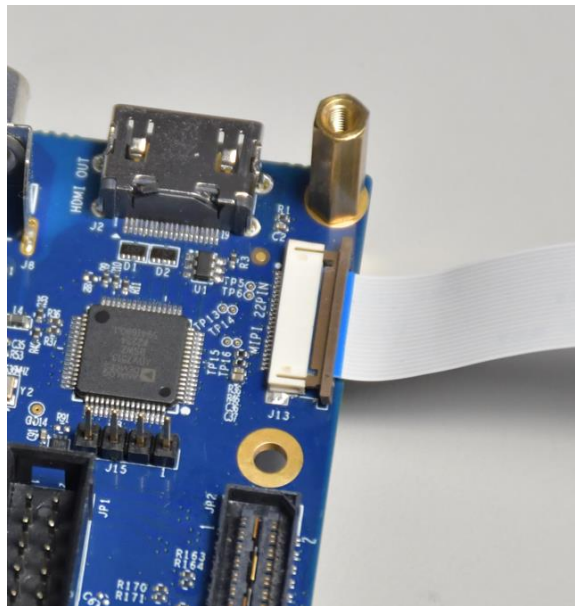


Figure 3-3 Insert the cable

3. Slide the locking bar forward (towards the cable) to lock it.

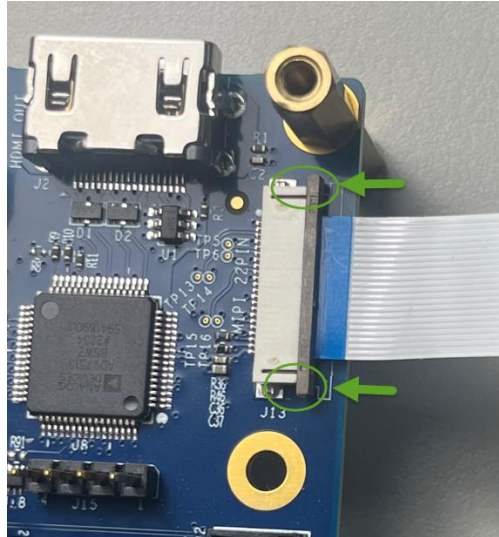


Figure 3-4 Lock the FPC connector's slider-lock

Chapter 4

VVP Based Example Codes

This chapter provides VVP (Video and Vision Processing) Suite based examples for users to get started using the MIPI CSI-2 Camera Module. Nios V processor is used to configure VVP IP and camera module.

4.1 VVP_MIPI_CSI2_IMX519 Overview

This demonstration shows how to implement a MIPI CSI-2 Camera Module Demo on Agilex 5 FPGA board, such as Comet A13 Kit, Comet A65 Kit, Atum A5 and DE25-Standard Boards. The Altera VVP (Video and Vision Processing) suite is used to decoder Bayer pattern and display video on the HDMI monitor. The Nios V processor is used to configure two I2C devices on the Camera Module. These two devices are Image Sensor and VCM(Voice Coil Motor).

■ Function Block Diagram

Figure 4-1 shows the Function block diagram of the VVP_MIPI_CSI2_IMX519 demonstration. The CSI2_DPHY_SYS (implement in csi2_dphy_sys.qsys) system is used to get raw data from the MIPI CSI-2 camera module. The system includes Altera MIPI DPHY IP and CSI-2 IP. The CSI-2 output video format is AXI4 Video stream by 4 pixels in parallel. The video content is 10-bit raw data in Bayer pattern with resolution 1920x1080.

The SYSTEM (implement in system.qsys) contain NIOS V system and VVP_SYSTEM Subsystem. The VVP_SYSTEM (implemented in vpp_sysem.qsys) sub-system is developed based on Altera's Video and Image Processing (VIP) suite. The Demosaic IP is used to decoder Bayer Pattern to RGB video. Note, the Demosaic IP only supports Lite mode, so the other IP also be configure as lite mode to consistent with the Demosaic IP. The Pattern Generator IP is used for debug purpose for make sure HDMI Display work well when MIPI camera malfunction. The Switch IP is used to select input video source from camera or pattern generator (color bar). The Bits Per Color Sample IP is used to convert 10 bit color samples (30-bits RGB) to 8 bit color samples (24-bits RGB). The Pixel in Parallel IP is used to convert 4 pixel in parallel to 1 pixel in parallel. The Frame Buffer IP is used to work as frame buffer between Camera input and HDMI output. The IP is configured as a 1920x1080 frame buffer and LPDDR4 is used as physical memory buffer. The cvo and fr2cv IP are used to convert the video stream for HDMI display.

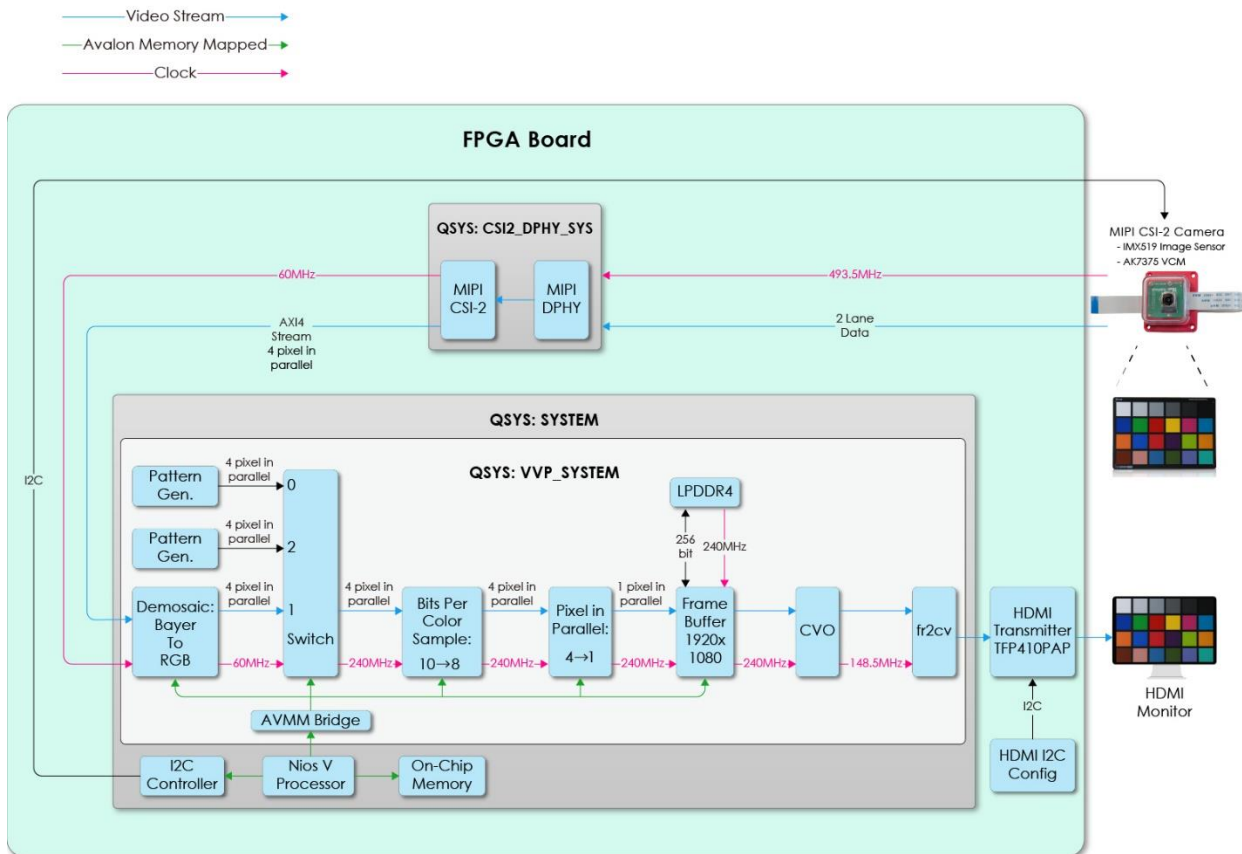


Figure 4-1 Block diagram of VVP_MIPI_CSI2_IMX519 demonstration

The NIOS V Processor is running on on-chip memory. In this demo, Nios V processor has two major tasks. First task is to configure the Image Sensor IMX519 and VIM (Voice Coil Motor) AK7375 in the MIPI CSI-2 Camera Module via I2C controller. The second task is used to configure the VVP IP via Avalon memory mapped interface. The Nios V Project is located in the software folder. The NIOS Program will show demo configuration menu for user to change register setting as shown **Figure 4-2**. **Table 4-1** shows the function detail about the menu.

```

===== Camera Demo Config Menu =====
[0]Camera: ReInit
[1]Camera: Exposure
[2]Camera: Color Balance
[3]Camera: Analog Gain
[4]Camera: Global Digital Gain
[5]Camera: Test Pattern
[6]Camera: Solid Test Pattern Color
[7]Camera: Dump Setting
[8]Focus: Set Position
[9]Focus: Scan
[10]VVP: Switch (0:color bar, 1: Camera, 2: SDI Pattern)
99: Quit
Please input your selection:|

```

Figure 4-2 Camera Demo Configuration Menu

Table 4-1 The functional keys of the digital camera demonstration

Menu	Function Description
[0]Camera: ReInit	Reconfigure image sensor register
[1]Exposure	Setup image sensor exposure time. Note, it will effect frame rate.
[2]Camera: Color Balance	Setup image sensor digital gain for red and blue channel.
[3]Camera: Analog Gain	Setup image sensor analog gain.
[4]Camera: Global Digital Gain	Setup image sensor global digital gain
[5]Camera: Test pattern	Enable/Disable Camera to output build-in test pattern.
[6]Camera: Solid Test Pattern Color	Setup color for Solid Test pattern.
[7]Camera: Dump Setting	Dump sensor major register setting.
[8]Focus: Set Position	Set VCM position for image focus.
[9]Focus: Scan	To adjust the VCM position, increase the value by 64 each time, starting from 0 and going up to 4095. This allows the user to scan for the optimal focus position.
[10]VVP: Switch	Specify Switch input channel. 1 for camera, 0 and 2 for VVP Patten generator.

■ The default camera settings

In this demonstration, the default camera settings are:

- Resolution: 1080P (1920x1080)
- Frame Rate: 60 fps
- Pixel Data: RAW10
- Mode: 2X2 Bayer Pattern

Users can change the settings base on their requirements.

■ Design Tools

- Quartus Pro V25.3
- Ashling RiscFree IDE for Intel FPGA V25.3

4.2 VVP_MIPI_CSI2_IMX519 for Comet A13 Kit

■ Demonstration Source Code

- Project directory: Demonstrations\VVP_MIPI_CSI2_IMX519
- Nios V project workspace: VVP_MIPI_CSI2_IMX519\software
- Demo batch file folder: VVP_MIPI_CSI2_IMX519\demo_batch

■ Demonstration Setup for Comet A13 Kit

1. Connect a USB Type-C cable between the host PC and the USB connector (J4) on the Comet A13 Carrier board.
2. Connect MIPI CSI-2 Camera Module to MIPI Connector (J7) on Carrier board.
3. Connect the HDMI output port (J3) on the Carrier board to a HDMI monitor (See **Figure 4-3**).
4. Power on the Carrier board.
5. Execute the demo batch file “test.bat” under the batch file folder VVP_MIPI_CSI2_IMX519\demo_batch.
6. The HDMI monitor will start showing the video captured from the camera.
7. Nios V terminal will show the demo configuration menu as shown in **Figure 4-2**.
8. **Table 4-1** summarizes the functional keys.

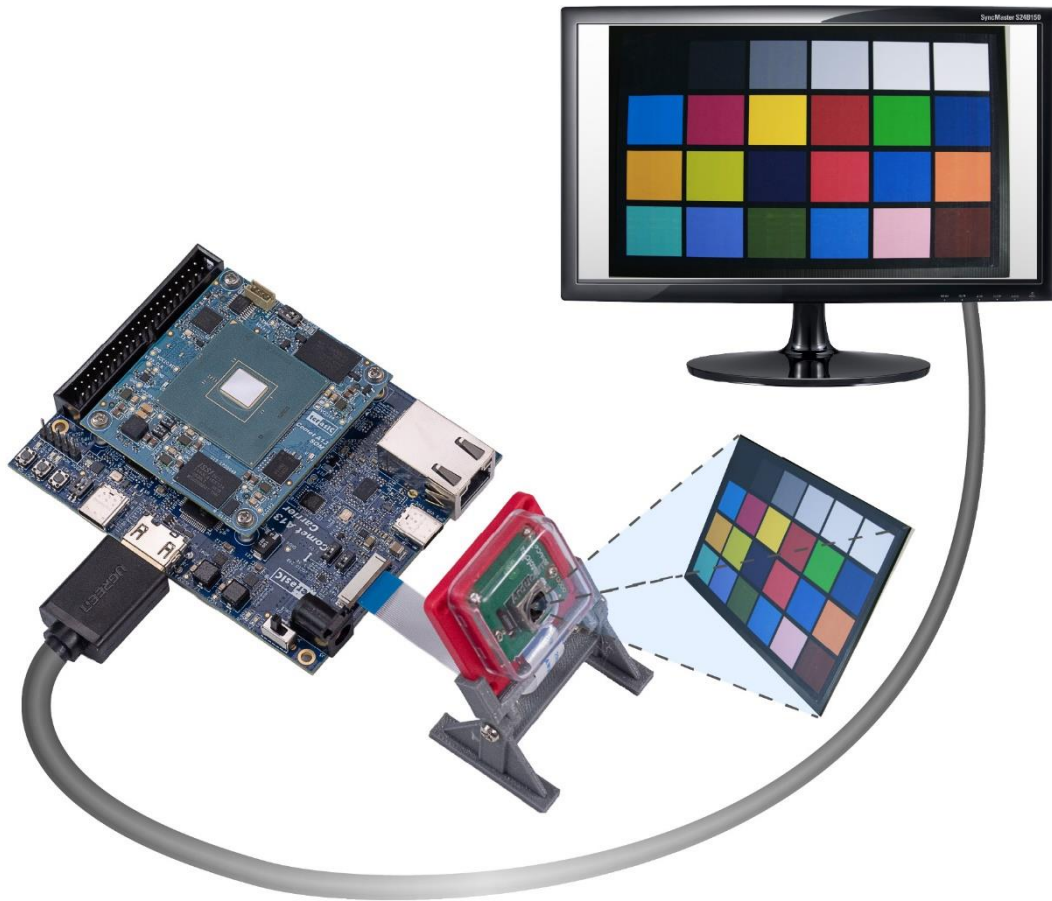


Figure 4-3 VVP_MIPI_CSI2_IMX519 demonstration setup for Comet A13 Kit

Chapter 5

Additional Information

5.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ **Terasic Technologies**

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Comet A13 Kit Web: comet-a13.terasic.com

■ **Revision History**

Date	Version	Changes
2026.01	First publication	
2026.07	V1.1	Change fan connector on SoM module from 3-pin to 4-pin